ALIDCT Inverse Discrete Cosine Transform Core

Application Notes

Rev. [6/2012]

6-20-2012

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General Information

The ALIDCT Application Notes contains description of the ALIDCT core architecture to explain its proper use.

ALIDCT soft core is the unit to perform the Inverse Discrete Cosine Transform (IDCT). It performs two-dimensional 8 by 8 point IDCT for the period of 64 clock cycles in pipelined mode.

Features

Key features

- Up to 85 MHz sampling frequency, 64-cycle calculation period,
- 1114 CLB slices,
- 12-bit input data,
- 9-bit coefficients,
- 8-bit results,
- pipelined mode,
- structure optimized for Xilinx XC4000, Virtex™, SpartanII™ FPGA devices.

Design features

IDCT core is intended for transforming data compressed by the Discrete Cosine Transform (DCT) into the initial image data format.

The characteristics of the IDCT make it extremely suited for image compression-decompression algorithms. IDCT reconstructs the image frame, which was coded by the Discrete Cosine Transform (DCT). Therefore IDCT is used in JPEG and MPEG standards of image compression-decompression procedures.

In general, the two-dimensional IDCT transforms an $n \times n$ data array into an $n \times n$ result array. First the IDCT transforms the columns then it transforms the rows.

The 8-point IDCT is calculated due to the equation

$$Y(m) = \frac{1}{2} \sum_{k=0}^{7} X(k) \cos \frac{(2m+1)k\pi}{16}, \quad m=0,1,...,7,$$

where $Y(k)$ is k th IDCT coefficient.

In most cases the input 8x8 image data block consists of integers in the range from 0 to 255. And before the DCT calculation the mean value 128 is subtracted from input data to minimize the redundancy in the input data block. In this case, after the IDCT calculation this mean value 128 must be added to input data to finish the image reconstruction.

The DCT transform can be implemented by ALDCT core supplied by Aldec.

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- **Highly pipelined calculations**

The input data arrays 8x8 are loaded in data by data manner with the period which is equal to the clock period. The output data arrays are outputted in the similar manner. Any time threschold between data arrays can be absent as well as high maximum clock frequency of the core is due to the pipelined calculations.

The delay between first data input and the first data output is equal to 182 clock cycles. The latent period of calculations is equal to 64 clock cycles.

- **High precision computations**

The quality of decoded image depends on the computation precision, for example, when photographic picture decompression. Different two-dimensional IDCT algorithms and implementations are different in computation precision. This core has 8-bit output data width, the maximum error does not exceed 1 least significant bit. The quadratic mean error is equal to 0.55 least significant bit.

The customer can select the needed output data width using proper generic constant.
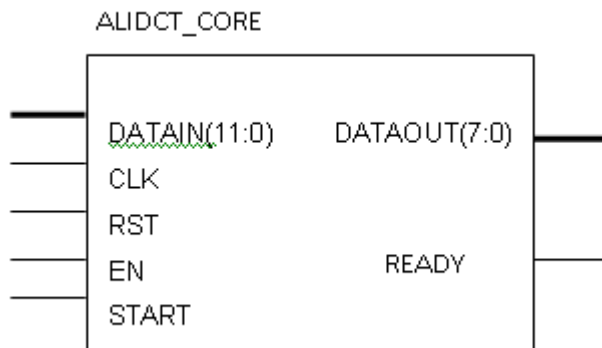
Interface

Symbol
Figure1 shows ALDCT core symbol.

Figure 1. ALIDCT symbol.

Signal description

The descriptions of the core signals are shown in the table 1.

SIGNAL	TYPE	DESCRIPTION
CLK	input	Global clock
RST	input	Global reset
START	input	IDCT start
EN	input	Clock enable
DATAIN[11:0]	input	Input data
DATAOUT[7:0]	output	Output data
READY	output	Result ready strobe

Table 1. ALIDCT core signal description.

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Data Format

Input data are 12 bit wide two's complement integers.

Output data are 8 bit wide two's complement integers. According to the IDCT formulas the magnitude of the output signal can be increased in 8 times comparing to the input signal magnitude. In the core the additional scaling factor 1/128 is used to support the proper output data width. Therefore, when the input signal is changed in range –2048 to 2047 then the output signal is changed in range –128 to 127. Depending on the generic constant SIGNED_DATA output data can be considered as signed or unsigned one. When unsigned, from all data the mean value 128 is added. As a result, when using DCT core with unsigned input data, the result after such IDCT will be the same as input data.

The core is intended to compute the transform, which is inversed to the DCT. When the input data is the result of the proper DCT then the output data of the IDCT core have minimum computational errors. For example, if the input data matrix consists of the sample (0,0), which is equal to 2047, and the rest of samples are is equal to 0 (such data represents the white field spectrum) then the resulting data matrix contains samples equal to 127.

When the input data is the random one then overflows can occur which force substantial errors. To minimize these errors the output data are saturated, i.e. the value which is greater than 127 is substituted by 127, a value which is less than -128 is substituted by 128.

To support the high precision, used for example in JPEG, the core can have up to 12-bit output data width. In this situation, up to 4 least significant bits can be added to the output bus.

Typical Core Interconnection

Typical core interconnection is shown on figure 2.
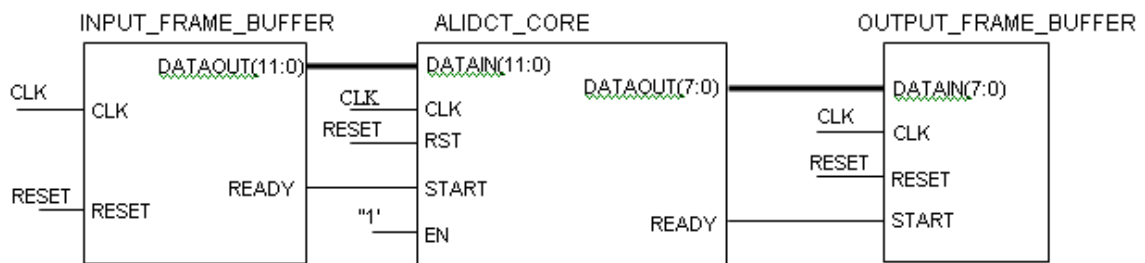

Figure 2. Core interconnection

Components:

 ALIDCT_CORE – ALIDCT core

INPUT_FRAME_BUFFER – RAM buffer which loads 8x8 blocks of DCT coefficients into IDCT core in row by row mode

OUTPUT_FRAME_BUFFER – RAM buffer which stores 8x8 blocks of IDCT results in row by row mode

Block Diagram

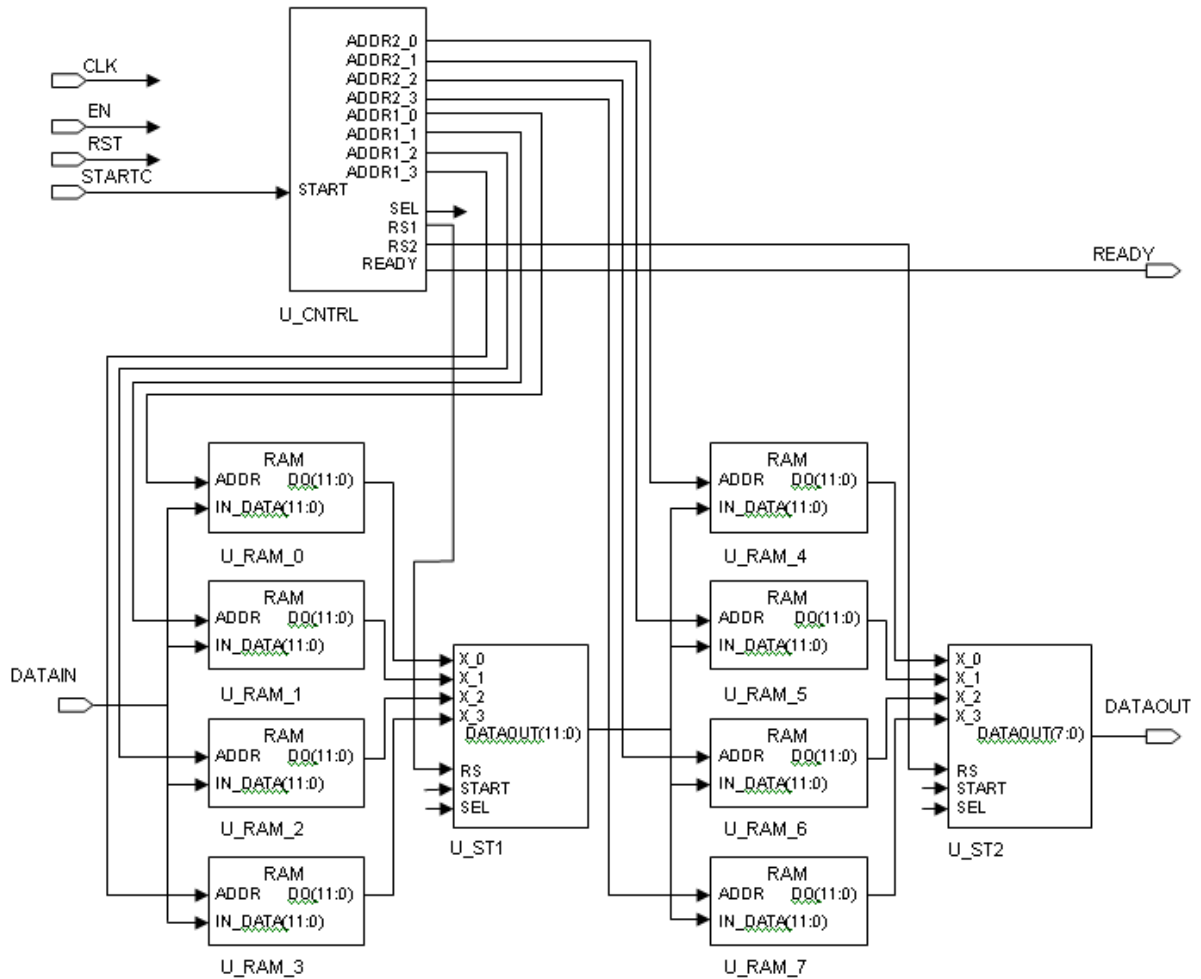The block diagram of the ALIDCT_CORE is shown in the fig.5.

Figure 3. Block diagram of the ALIDCT core

Components:

- U_RAM_0,…, U_RAM_7 – data RAMs, each of them is of 32 words of volume,
- U_ST1, U_ST2 – stages which implement 8 point IDCTs for columns, and rows, respectively
- U_CNTRL – control unit which generates control and address signals

Note: the connections of signals CLK, RST, START, EN, SEL, are not showed on the figure 3.

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Implementation Data

Performance

The table 2 shows the ALDCT core performance in Xilinx XC4000 and VIRTEX™ devices for 8 bit output data, respectively.

Target device	XC4028XLA-07	XCV100-6	XCV100E-8
Area, CLB, CLB slices	947	918	918
Area, equivalent gates	27165	36784	36784
System clock, and maximum sampling frequency fmax	51 MHz	84 MHz	108 MHz

Table 2. Implementation Data for 8 bit accuracy

Timing diagram

To run the IDCT core the START signal is activated for minimum one clock period. After falling edge of the START impulse the input data are sampled in the port DATAIN. Each data is sampled in each clock cycle by the rising edge of the clock signal. The block 8x8 of data is inputted in the row-by-row order beginning from the row zero, column zero data. When 64 data are sampled, the DCT transform begins running. When 182 clock cycles are passed from the START impulse, the output impulse READY shows that the IDCT is finished. After falling edge of the READY impulse the output data are outputted in the port DATAOUT in the similar order as input data are sampled.
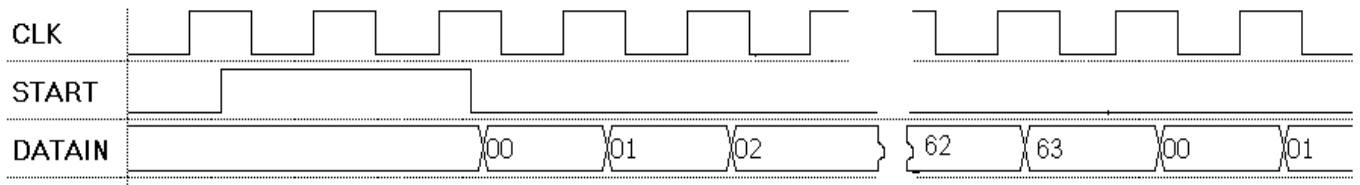

Figure 4. Input data sampling diagrams

The input data sampling is shown on the fig.4, and the result output process is illustrated on the fig.5.
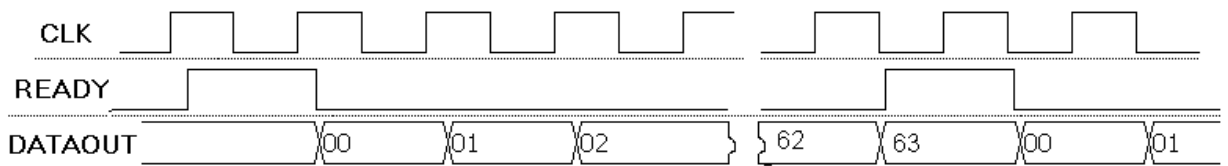

Figure 5. Result output diagrams

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The time delay from the signal START to the last result output is equal to 182+64=246 clock cycles. Therefore, this figure is equal to the DCT calculation time for one data block. The signal START must be synchronous one relatively to the signal CLK.

The ALIDCT core can calculate a group of data blocks in the pipelined mode. In this mode the START impulse is activated once per group of data blocks. Each data block is sampled without time thresholds between blocks. Each block of results is followed by the READY impulse. Therefore, in pipelined mode the core calculates the IDCT transform approximately for 64 clock cycles when the block number is rather high.

The high level of the signal EN enables operation of the DCT core, and can be used to slow-down the core when it is used with slow signal sources.

Deliverables

The ALIDCT core is delivered as a set of VHD files:

- ALIDCT.VHD – root file of the synthesable core model.
- STAGE1.VHD, STAGE2.VHD, MUL_C.VHD, MUL_C1.VHD, MUL.VHD, MUL11.VHD, RAM.VHD- files of the component models.
- ALIDCT_BEH.VHD – file of the behavioral core model which implements floating point arithmetic.
- Test bench files TEST_ALDCT.VHD, BMP_GENERATOR.VHD, COMPARE.VHD.
- Example of the ALIDCT core after synthesis, and its timing model.